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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,003	03/30/2004	Ja-Hum Ku	2421-000037/US	2675

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EXAMINER	
LEE, CHEUNG	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/812,003	KU ET AL.
	Examiner	Art Unit
	Cheung Lee	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-22* is/are allowed.

6)☒ Claim(s) *1,23,24 and 26-35* is/are rejected.

7)☒ Claim(s) *2-11,25 and 36-40* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

HA NGUYEN
PRIMARY EXAMINER

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Notice to Applicant

1. Applicants Amendment and Response to the Office Action mailed on November 3, 2005 has been entered and made of record.

Response to Amendments

2. In view of applicants' amendment to the specification, the objections to the specification have been withdrawn. However, the examiner suggests to remove the paragraph of the "Cross Reference to Related Application" to avoid any confusions.

3. In view of applicants' amendments to the claims, the objection to claims 10-11, 21-22 and 34-36 has been withdrawn.

4. In view of applicants' arguments and amendments to the claims 1-40 under 35 U.S.C. 112, the rejection of the claims has been withdrawn.

5. In view of applicants' amendments and arguments filed on February 3, 2006, the rejections of claims 1, 23, 24-36 under 35 U.S.C. 103(a) as stated in the indicated Office Action have been withdrawn. Applicants' arguments have been rendered moot in view of the new or modified ground of rejection given below.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 23-24 and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine et al. (US Pat. 6339018; hereinafter "Ballantine") in view of Wolf et al. (NPL, "Silicon Processing for the VLSI Era", Volume 1, hereinafter "Wolf ").

7. With respect to claim 1, referring to figures 1-7, Ballantine discloses a method of forming a semiconductor device comprising, in order: implanting a dopant into a substrate 300 to form a source/drain region 345 (step 235); forming a silicide blocking layer 350 on the substrate (step 240); exposing silicon surfaces on the substrate (step 245); forming silicide layers 355 on the exposed silicon surfaces (step 250; see fig. 3F), the silicide layers being formed at a silicidation temperature T_s (col. 5, lines 28-35), but Ballantine does not disclose expressly wherein annealing the substrate to activate a portion of the dopant, the annealing being conducted at an anneal temperature T_a, wherein $T_s < T_a$.

Wolf discloses a temperature range, which is 1000-1200°C, to activate of implanted impurities such as As, P, and B by rapid thermal processing (page 305, lines 5-7). Since most as-implanted impurities do not occupy substitutional sites, a subsequent thermal step is employed to bring about electrical activation (page 303). And the activation annealing process is done before the silicidation process because of instability of the $TiSi_2$ above ~900°C (page 399). In addition, it would have been obvious to perform annealing process after forming the silicide blocking layer to avoid any possible deactivation of the activated dopants while forming the silicide blocking layer.

At th e time of the invention it would have been obvious to a person of ordinary skill in the art to perform annealing process, as taught by Wolf.

The motivation for doing so would have been to activate the implanted impurities (Wolf, page 303).

8. With respect to claim 23, referring to figures 1-7, Ballantine discloses a method of forming a semiconductor device comprising, in order: forming an active region (steps 205 and 210) in a semiconductor substrate 300, forming a STI region 310A will distinguish the active region; forming a gate electrode 330 structure in the active region (steps 220 and 225); implanting a first dopant into the active region adjacent the gate electrode structure, Ballantine discloses an implantation of a source/drain extension 345A or a lightly doped drain (LDD) before forming a spacer 340 (col. 6, lines 8-16); forming spacers 340 adjacent the gate electrode structure (step 230); implanting a second dopant into the active region adjacent the spacers (step 235); forming a silicide blocking layer 350 on the substare (step 240); exposing a silicon surface on the substrate (step 245); forming a metal layer in direct contact with exposed silicon surface (see fig. 3F; step 250); and reacting the metal layer with the exposed silicon surface to form a silicide layer 355 on the silicon surface at a silicidation temperature T_s (col. 5, lines 28-35), but Ballantine does not disclose wherein annealing the substrate to activate a portion of the dopant, the annealing being conducted at an anneal temperature T_a, wherein $T_s < T_a$.

Wolf discloses a temperature range, which is 1000-1200°C, to activate of implanted impurities such as As, P, and B by rapid thermal processing (page 305, lines 5-7). Since most as-implanted impurities do not occupy substitutional sites, a subsequent thermal step is employed to bring about electrical activation (page 303). And the activation annealing process is done before the silicidation process because of

instability of the $TiSi_2$ above ~900°C (page 399). The arguments and motivation stated in claim 1 also apply.

9. With respect to claim 24, Ballantine in view of Wolf discloses wherein forming the silicide layers includes depositing a metal layer on the exposed silicon surfaces (Ballantine, step 250), the metal layer being capable of forming a silicide at a silicidation temperature of less than 700°C (Ballantine, col. 5, lines 28-35).

10. With respect to claim 26 and 27, Ballantine in view of Wolf does not disclose expressly wherein [Claim 26] the silicide blocking layer is formed at a temperature T_{bl} that is below about 830°C; and [Claim 27] T_{bl} is between about 535 and about 825°C. However, any variation in the temperature for forming the silicide blocking layer in the present claim is obvious in light of the cited art, because the changes in the temperature for forming the silicide blocking layer produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

11. With respect to claim 28, Ballantine in view of Wolf does not disclose expressly wherein the silicide layer is formed at a temperature T_s that is between about 400 and about 530°C. However, any variation in the temperature for forming the silicide layer in the present claim is obvious in light of the cited art, because the changes in the temperature for forming the silicide layer produce no unexpected function. The routine varying of parameters to produce expected changes are within the ability of one of ordinary skill in the part. Patentability over the prior art will only occur if the parameter

variation produces an unexpected result. *In re Aller, Lacey and Hall*, 105 USPQ 233, 235. *In re Reese* 129 USPQ 402, 406.

12. With respect to claim 29, Ballantine in view of Wolf discloses wherein the substrate is annealed at a temperature T_a that is at least about 830°C (Wolf, page 305, lines 5-7).

13. Claims 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine in view of Wolf, as applied above, and further in view of Ku et al. (US Pat. 6329276; hereinafter "Ku").

Ballantine in view of Wolf does not disclose expressly wherein [Claim 30] forming a capping on the metal layer before reacting the metal layer with the exposed silicon; and [Claim 31] the capping layer includes a major portion of titanium nitride.

Ku discloses forming a capping layer by depositing titanium nitride on a metal layer before silicide heat treatment (col. 3, line 56-col. 4, lines 2).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use a capping layer on the silicide metal layer, as taught by ku.

The motivation for doing so would have been to prevent oxidation and overgrowth of silicide metal into an unintended area (Ku, col. 3, lines 62-65).

14. Claims 32-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ballantine in view of Wolf, as applied above, and further in view of Cabral, JR. et al. (US Pub 2004/0123922; hereinafter "Cabral").

15. With respect to claims 32 and 33, Ballantine in view of Wolf does not disclose wherein [Claim 32] the metal layer is nickel alloyed with one or more minor metals, the minor metals being selected from a group consisting of tantalum, vanadium, zirconium, hafnium, tungsten, cobalt, platinum, chromium, palladium, niobium and combinations thereof, wherein the minor metals constitute no more than about 20 atomic percent of the metal layer; and [Claim 33] the minor metal is tantalum and is present in a concentration of between about 0.1 and about 10 atomic percent of the metal layer.

Cabral discloses Ni alloying additives preferably include Ta, W, Re or mixture thereof (page 2, paragraph 35), and the most preferable amount of the alloying additive in the Ni alloy layer is from 0.5 atomic % to 10 atomic % (page 3, paragraph 38).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to use Ni alloy and alloying additives as silicide metal, as taught by Cabral.

The motivation for doing so would have been to obtain Ni monosilicide contacts, which consume less Si than conventional Ti or Co silicide contacts, and to stabilize the Ni monosilicide phase (Cabral, page 1, paragraph 5; page 2, paragraph 32).

16. With respect to claims 34 and 35, the combine teaching of Ballantine, Wolf and Cabral discloses wherein [Claim 34] $T_s < 550^{\circ}C$ (Cabral, page 3, paragraph 44) and $T_a > 750^{\circ}C$ (Wolf, page 305, lines 5-7); and [Claim 35] T_s is between about 400 and about $530^{\circ}C$ (Cabral, page 3, paragraph 44), and T_a is between about 830 and about $1150^{\circ}C$ (Wolf, page 305, lines 5-7). In the case where claimed ranges "overlap or lie inside rages disclosed by the prior art" a prima facie case of obviousness exists. *In re Wertheim*, 541 F. 2d 257, 191 USPQ 90 (CCPA 1976); *In re Woodruff*, 919 F. 2d 1575,

16 USPQ 2d 1934 (Fed. Cir. 1990). And when the silicide annealing process is performed at a temperature less than 550°C, the claimed limitation is met.

Allowable Subject Matter

17. Claims 12-22 are allowed.

The following is an examiner's statement of reasons for allowance: claim 12 recites annealing the substrate to form activated dopant in the source/drain region; forming a silicde blocking layer on the substrate, thereby deactivating a portion of the activated dopant; and annealing the substrate to reactivate a portion of the deactivated dopant. These features in combination with the other elements of the claim are neither disclosed nor suggested by the prior art of record.

Claims 13-22 depend from claim 12, so they are allowed for the same reason.

18. Claims 2-11, 25 and 36-40 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: claim 2 recites reacting the nickel alloy layer with the exposed silicon surface to form a nickel silicide layer having an upper layer and a lower layer, wherein the alloying metal is preferentially segregated in the upper layer. Claim 25 recites activating the first and second dopants prior to forming the silicide blocking layer to form activated dopants, wherein the formation of the silicide blocking layer tends to deactivate a portion of the activated dopants. Claim 36 recites the capping layer has a nitrogen:titanium atomic ratio of at least about 0.5. Claim 37 recites the silicide layer

includes a lower layer and an upper layer, the lower layer having a first thickness and the upper layer having a second thickness, and further wherein the first thickness is at least 70% of a sum of the first thickness and the second thickness. These features in combination with the other elements of the claims are neither disclosed nor suggested by the prior art of record.

Claims 3-11 and 38-40 variously depend from claims 2 or 37, so they are allowed for the same reason.

Conclusion

Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheung Lee whose telephone number is 571-272-5977.

The examiner can normally be reached on Monday through Friday from 8:30AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cheung Lee

April 13, 2006

HA NGUYEN
PRIMARY EXAMINER